REMARKS

Reconsideration of this patent application is respectfully requested in view of the foregoing amendments, and the following remarks.

It is noted that the previously made Restriction Requirement has been repeated and has now been made Final.

The Patent Examiner has stated that the subject matter of this patent application admits of illustration by a drawing to facilitate understanding of the invention. Applicant is required to furnish a drawing under 37 CFR 1.81.

Hence a proposed drawing showing FIG. 1 and a proposed Amendment to the Specification on pages 16 and 17 describing this drawing are enclosed herewith. No new matter has been introduced into the required drawing, or into the Specification.

Claim 1 has been rejected under 35 U.S.C. 103(a) as being unpatentable over *Wilson et al (U.S. Patent No. 6,284,384) and*

Vepa (EPA No. 684634), cited by the Applicants' in their IDS.

The present invention comprises an epitaxially coated semiconductor wafer which, prior to the deposition of the epitaxial layer, experienced a stock removal polishing step only and which has a surface roughness of 0.05 to 0.29 nm RMS, measured by AFM on a 1 μm - 1 μm reference area; and wherein a surface of the epitaxial layer has a maximum density of 0.14 localized light scatters per cm^2 with a cross section of greater than or equal to 0.12 μm.

The *Wilson U.S. Patent No. 6,284,384* discloses only that the wafer is subjected to polishing techniques which are well known in the art before the epitaxial layer is deposited and the reference lacks any teaching as to the surface roughness.

More particularly, the *Wilson U.S. Patent No. 6,284,384* in column 7 lines 65 to 67 to column 8 lines 1 to 7 discloses a single crystal silicon wafer comprising a surface having an epitaxial silicon layer deposited thereon. The epitaxial surface of the wafer typically has an average light scattering event concentration of no greater than about 0.06/cm^2, as measured by a

laser-based auto inspection tool configured to detect light scattering events corresponding to polystyrene spheres having diameters of no less than about 0.12 μm.

See *Wilson* in column 4 lines 60 to 65 and also in column 5 lines 46 to 51.

The Patent Examiner has stated in this Office Action that *Wilson* does not specifically describe that the front surface of the wafer prior to the deposition of epitaxial layer, has a surface roughness of 0.05 to 0.29 nm RMS, measured by AFM on a 1 Ux1Um reference area.

The deficiencies in the teachings of the primary reference to *Wilson* are not overcome by the secondary reference to *Vepa*.

Vepa on page 3 in lines 45 to 51 discloses that a semiconductor wafer can be polished using a two step stock removal phase on the same polisher before finish polishing the wafer. The resultant polished semiconductor wafer has less surface roughness than a conventional wafer and can be polished

as quickly. The wafers rough polished by the method of *Vepa* exhibit an average surface roughness of less than 1.0 nm Ra as measured on a 1 mm x 1 mm scan with an optical interferometer.

More particularly, *Vepa EP-684634 A2*, which is also mentioned on page 3 of the Specification of the present patent application, discloses that the surface roughness of a semiconductor wafer can be less than 1.0 nm Ra as measured on a 1 mm - 1 mm scan. However, this surface roughness is achieved by applying the wafer to an expensive two step stock removal polishing. Moreover, the roughness value disclosed in the *Vepa* reference is measured on a 1 mm x 1 mm scan area measured with an optical interferometer. Hence this measurement of *Vepa* is not comparable to the claimed value which recites a lateral resolution of 1 μm x 1 μm measured with an atomic force microscope, AFM.

For all these reasons, elected claim 1 is believed to be patentable under 35 U.S.C. 103 over all the prior art applied by the Patent Examiner. A prompt notification of allowability is respectfully requested.

Respectfully submitted,

SIEBERT ET AL - 2

COLLARD & ROE, P.C.
1077 Northern Boulevard
Roslyn, New York 11576
(516) 365-9802

Allison C. Collard, Reg.No.22,532
Edward R. Freedman, Reg.No.26,048
Attorneys for Applicant

ERF/mt

Enclosures: (1) Marked-Up Version of Amended Specification;
(2) Proposed Drawing FIG. 1.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231, on August 12, 2002.

Lisa L. Vulpis

MARKED-UP VERSION
OF
AMENDED SPECIFICATION

An epitaxially coated semiconductor wafer produced according to the invention, in particular a silicon wafer with an epitaxial silicon coating, fulfills the requirements for the production of semiconductor components with line widths of less than or equal to 0.18 µm. The process according to the invention has proved to be an optimum solution for the production of epitaxially coated silicon wafers having the features outlined above. The geometry requirements imposed on the starting material are minimal, which reduces the demands imposed on the preliminary processes. The excellent wafer geometry which is obtained in the two-sided polishing is produced even after relatively little material has been removed. By virtue of the enhanced process reliability, together with a reduced risk of fracture, the wafers of the invention are produced in very high yields without cost-intensive steps for local geometry correction, for example by plasma etching, being necessary. This excellent wafer geometry is also completely preserved on the end product according to the invention as a result of the need to carry out a final polishing step being obviated.

18

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows

19

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be further described by reference to the following examples which are not to be deemed limitative of the present invention in any manner thereof.

All the examples and comparative examples described below relate to the production of silicon wafers with a diameter of (300±0.2) mm, an oxygen content of $(6\pm1)\cdot10^{17}$ atoms/cm^3, and a boron doping which leads to a resistance in the range from 5 to 20 mΩ·cm, and which have an epitaxial silicon layer on the front surface with a boron doping which leads to a resistance in the range from 1 to 10 Ω·cm.

Referring to FIG. 1,

EXAMPLE (INVENTION)

300 mm silicon wafers with double-side polished surface, which had been polished and cleaned as described in steps (a) and (b), were available for this example. The roughness of the prepolished wafer was 0.7 nm RMS (AFM, 1 µm × 1 µm).

Step (c): the front surface of the semiconductor wafers was then subjected to a pretreatment prior to the epitaxial coating in the epitaxy reactor, with the aim of, in a first step, removing the native oxide on the front surface and, in a second step, drastically reducing the roughness on the surface, so that after epitaxial coating a semiconductor wafer with considerably improved properties in terms of surface roughness and number of localized light scatterers is available. This was achieved by the fact that, firstly, the native oxide was removed in a hydrogen atmosphere at